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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/618,039	07/11/2003	Trevor J. Bauer	X-1097-1D US	4121

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EXAMINER	
ENGLUND, TERRY LEE	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 02/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/618,039	BAUER, TREVOR J.	
	Examiner	Art Unit	
	Terry L Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07112003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The abstract of the disclosure is objected to because the phrasing "has N pass gates" on line 3 can be considered misleading and/or inaccurate. For example, from the applicant's own disclosure and figures, it is clearly understood that each pass gate multiplexer circuit comprises 2N pass gates. Therefore it is suggested that the phrase be amended to indicate the circuit has --2N pass gates--, --N pass gate pairs--, or --N first pass gates, N second pass gates,--. Correction is required. See MPEP § 608.01(b).

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-17 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over respective claims 1-17 of U.S. Patent No. 6,617,912 B1 (cited on the accompanying PTO-892 to ensure it is clearly documented with respect to the present application). Although the conflicting claims are not identical, they are not patentably distinct from each other because the patent's specific use of "N" has now been replaced within the present application's claims with the broader "a plurality of" (or "the plurality of"). For

example, the patent's independent claim 1 recites "N input circuits", "N is an integer greater than four", and "N memory cells", thus specifically indicating more than four of each item, and also that there is an equal number of each item. The patent's independent claims 6 and 11 use some variations of those phrases such as "N input terminals", "N first pass gates", "N second pass gates", and/or "N configuration memory cells." However, in the present application's claims, the broader recitation "plurality of" allows circuitry that has two or more of the claimed items, wherein the number of memory cells does not have to be equal to the number of input circuits (or to the number of first or second pass gates). Therefore, the claims of the present application read on the claims of the patent.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-10 are also rejected under 35 U.S.C. 102(b) as being anticipated by Young, a reference cited on both the applicant's IDS, and the applicant's related U.S. Patent 6,617,912 B1. Fig. 4 shows a multiplexer circuit comprising a plurality of input circuits (e.g. 6: T0- to T5-), each input circuit comprising an input terminal (e.g. IN0 to IN5, respectively), first pass gate (e.g. T0A,T1A,T2B,T3A,T4A,T5A), and second pass gate (e.g. T0B,T1C,T2C,T3C,T4C,T5B), wherein a common output node OUT is coupled to the output terminals of each input circuit. The circuit also shows a plurality of memory cells (e.g. 3: MA to MC), with each memory cell being coupled to two pass gates in two respectively different input circuits (e.g. memory cell MA

has its inverted output coupled to first pass gates T0A/T1A of input circuits T0-/T1-) anticipating claim 1. [From the configuration shown in Fig. 4, it is known and understood that if one memory cell is upset, it will affect four pass gates/input circuits, and therefore four possible signal paths through the multiplexer. For example, if memory cell MA is upset, its signals /A and A will reverse their logic values affecting the operation of their respective pass gates T0A,T1A and T4A,T5A.] Although Fig. 4 does not show a buffer coupled to output node OUT, Fig. 6 clearly shows the output of multiplexers 61 and 62 coupled to buffers BUFA and BUFB, respectively. Therefore, it is understood that the reference does show/disclose the capability of coupling the output of a multiplexer, such as the one shown within Fig. 4, to its own respective buffer, anticipating claim 2. Young discloses the multiplexer could have 20 inputs (e.g. see columns 2 (lines 24-25) and 6 (lines 44-66)), and it is understood each input corresponds to it own input circuit (a pair of first/second pass gates) as shown in Fig. 4. Therefore, a 20-input multiplexer would have eight input circuits, thus anticipating claim 3. Also, since each of the pass gates is shown as an N-channel transistor, claim 4 is anticipated. Young discloses only two transistors in one signal path are used at any one time (e.g. see columns 2 (lines 30-56) and 3 (lines 55-64)), and since it is clear that each of the two pass gates within each input circuit is controlled by it own respective memory cell, then exactly two memory cells are configured to enable the associated pass gates (within the selected input circuit being used), anticipating claim 5. Interpreting Fig. 4 is a slightly different way, claims 6-10 are anticipated for the same reasons as described above with respect to claims 1-5. The difference being that independent claim 1 recites a plurality of input circuits, each having an input terminal, first and second pass gates, and an output terminal, wherein independent claim 6 describes a plurality of input terminals, an

output terminal, a plurality of first pass gates, and a plurality of second pass gates, wherein a series coupling of first/second pass gates form a pass gate pair between the associated input terminal and the commonly connected output terminal without specifically identifying the pair of first/second pass gates as an input circuit. Therefore, it is not deemed necessary to repeat the various connections and relationships (already described within claims 1-5) because one of ordinary skill in the art would recognize the varied differences between the recited limitations within claims 1-5 and 6-10, respectively.

No claim is presently allowable.

Allowable Subject Matter

However, claims 11-17 would be allowable if a timely filed terminal disclaimer is submitted. There is presently no strong motivation to modify or combine any prior art reference(s) to ensure the plurality of multiplexer circuits (as described) will programmably couple the plurality of interconnect lines to each other, as well as to the plurality of logic blocks, as understood from the limitations recited within independent claim 11, upon which claims 12-17 depend upon.

Prior Art

The other prior art reference on the accompanying PTO-892 is cited for interest and documentation purposes. Since this other reference also has the same inventor and assignee as the present application, and U.S. Patent 6,617,912 B1 cited above with respect to the double patenting rejections, no copy of this reference is being submitted to the applicant. The Prior Art Fig. 1 of this other reference is clearly disclosed as a "type of circuit commonly included in FPGA interconnect structures" (e.g. see column 1, lines 51-57). The figure shows a plurality of

input circuits (e.g. 115,123; 111,122; 106,121; and 102,120) each comprising a corresponding input terminal (e.g. IN15; IN11; IN6; and IN2) coupled to a respective first pass gate (e.g. 115; 111; 106; and 102). Each input circuit also comprises a second pass gate (e.g. 123; 122; 121; and 120) coupled between its respective first pass gate and a common output node INT of the input circuit. Fig. 1 also shows a plurality of memory cells (e.g. M7 and M6) susceptible to single event upsets (e.g. see column 2, lines 46-48). Since memory cell M7 is coupled to the gate of two respective pass gates (e.g. 115 and 111) in different input circuits, and memory cell M6 is coupled to the gate of its two respective pass gates (e.g. 106 and 102), this other reference closely corresponds to all of the limitations recited within at least independent claims 1, and 6. Also, since each of the pass gates is an N-channel transistor, and buffer BUF is coupled to output node INT, the reference's Prior Art Fig. 1 also corresponds to the limitations recited within at least claims 2, 4, 7, and 9. Therefore, this other reference should be reviewed and considered with respect to the broad, basic independent claims of the present application.

The prior art references cited on the IDS submitted by the applicant were reviewed and considered. The Young reference was used in formal rejections described above. Of the other references, although they show an input circuit with two series coupled pass gates, these references do not clearly show or disclose each pass gate with its gate coupled to a respective memory cell. Instead, each gate is coupled to either a decoder, or to receive a logic signal from some unknown circuitry.

Any inquiry concerning this communication from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

TLE
Terry L. Englund

12 February 2004

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
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